REMARKS

This is a re-submission in response to a notice of a non-compliant amendment dated April 15, 2005, and another dated May 19, 2005. In the Office Action of January 14, 2005, made final, the Examiner objected to claims 1-7 for an informality in claim 1, rejected claims 9-13 under 35 U.S.C. 112, second paragraph as being indefinite, and rejected claims 1-18 under 35 U.S.C. 103 as being obvious. Claims 1-8 and 14-18 remain in the application.

The informality of claim 1 was for repeating a word. This has been addressed by amending claim 1.

The rejection for indefiniteness has been obviated by canceling claims 9-13. .

The Examiner largely reiterated the previous reasoning for the obviousness rejections and then concluded with two paragraphs that addressed applicants' response. Applicants accordingly also provide applicants' previous arguments and also a response to the Examiner's position with regard to applicants' previous response using the same order as the Examiner.

The Examiner's rejection for obviousness used Child as the primary reference. Child discloses a circuit that performs a single type of hash function (SHA) serially instead of applicants' parallel approach that can also selectively perform more than one type of hash function. Applicants' approach is both faster and requires less space on the integrated circuit.

With regard to claim 1, the Examiner used Childs and four additional references, Ober, Schneier, Turner, and Batcher, to come to conclusion that claim 1 was obvious to one or ordinary skill in the art. The claimed first multiplexer is useful in allowing for the use of the register file for both hash modes. The Examiner states that this claimed first multiplexer is obvious because multiplexers are known to switch between a signal and a reference and that this claimed location in the circuit is obvious because there is an incentive to minimize the number of elements. In effect the Examiner is saying two things: (1) one of ordinary skill in the art would recognize the benefit of applicants' invention and (2) anytime known elements are used to achieve a benefit that is recognizable to one of ordinary skill in the art, it is obvious for one of ordinary skill in the art to have done so. Applicants agree with the first but not the second. The Examiner's application of the legal requirement for an incentive to combine implies that anytime a circuit that uses transistors of the type known in the art for switching or amplification and such circuit provides a known desired benefit such as reducing circuit elements or improving speed, such circuit is obvious and unpatentable. In this case there is no suggestion in the prior art that

the elements that are combined by Applicants can be combined in the manner claimed by Applicants. Ober teaches that both hash functions can exist on the same integrated circuit, but applicants have not been able to find any reference that there is any suggestion that these two functions can share the same circuitry much less teach which elements can be shared. The Examiner is applying hindsight using Applicants' teaching to construct from the prior art the resulting claimed circuits. Accordingly, applicants submit that claim 1 patentably distinguishes over the five reference combination applied by the Examiner.

With regard to claims 2-7, the Examiner continued to apply the same approach that because Applicants used known circuit elements in achieving the result and the result was beneficial, the result was obvious. Applicants disagree as stated above.

Independent claim 8 claims an adder with a first, second, third, fourth, and fifth input. Childs discloses a two input adder 522. Notice that applicants' circuit does not require multiplexer 501 and flip-flops 502-506. Childs needs these flip-flops as temporary storage for chaining variables. This makes the operation significantly slower. Further, these flip-flops require more space than the additional space required over a two input adder. Also multiplexer 520 is not required and accumulator 523 is not used. There are multiplexers used to control the inputs to the five input adder, but these are for the different modes, SHA-1 and MD5. Once the mode is selected these multiplexers simply feedthrough the input for that mode. There is no switching between inputs to the adder during the determination of the hash output. In Childs, multiplexers 521 and 520 are switching inputs (serial approach) to adder 522 during the determination of the hash output, thus being significantly slower in determining the hash output than applicants' five input adder (parallel approach) manner of performing the hash function. Accordingly, applicants submit that claim 8 is patentably distinct from the art cited by the Examiner.

With regard to claims 9-13, the Examiner continued to apply the same approach used against claim 1 that because Applicants used known circuit elements in achieving the result and the result was beneficial, the result was obvious. Applicants disagree as stated above.

With regard to independent claim 14 and dependent claims 15-18, the Examiner used the same type of argument used in against claim 1. Applicants disagree with this reasoning as per the response for claim 1.

With regard to claim 15, Applicants submit that element 603 of Childs is not a decoder and thus is not appropriate as being asserted as being analogous to the claimed decoder of claim 15.

Further with regard to claim 16 as amended, the analogy used by the Examiner is not a correct representation of the prior art. The Exclusive Or claimed is not analogous to that of Childs 605.

With regard to the Examiner's new portions of the response, the analysis of claim 8 was altered but still used the same approach used previously and used in rejecting other claims. The Examiner's view of his analysis regarding all of the claims is that hindsight engineering is ok so long as it is not only taught by applicants and cited *In re McLauglin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971). In this regard, most of the claimed connections are only taught by applicants so the Examiner's view of that holding does not help the Examiner's case. The Examiner's approach has been to start with applicants' invention and the advantage thereof and see if the various claim elements exist in the prior art and see if one ordinary skill in the art would have been able to use the prior the art to achieve applicants invention after having seen applicants invention and would understand there is a benefit. Under this test it's difficult to imagine that there is any circuit that uses only known elements such as transistors, resistors, and capacitors that would be patentable. The proper test is that the prior art itself must provide the motivation to combine not that one of ordinary skill in the art would be able to build applicants' invention and appreciate its benefits after having been taught applicants' invention. Accordingly, applicants submit that the rejection of claims 1-18 is improper because of the improper analysis of the Examiner.

No amendment made was related to the statutory requirements of patentability unless expressly stated herein. No amendment made was for the purpose of narrowing the scope of any claim, unless Applicant has argued herein that such amendment was made to distinguish over a particular reference or combination of references.

Applicants believe the application is in condition for allowance which action is respectfully solicited. Please contact the below-signed if there are any issues regarding this communication or otherwise concerning the current application.

Respectfully submitted,

SEND CORRESPONDENCE TO:

Freescale Semiconductor, Inc.
Law Department

Customer Number: 23125

By: James L. Clingan Jr.

James L. Clingan, Jr.
Attorney of Record
Reg. No.: 30,163
Telephone: (512) 996-6839
Fax No.: (512) 996-6854